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10/765,897	01/29/2004	Chih-Yung Chen	32052-8721.US	2606

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EXAMINER	
DOAN, DUC T	

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2185	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/765,897	CHEN ET AL.	
	Examiner	Art Unit	
	DUC T. DOAN	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 August 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Status of Claims

Claims 1-20 have been presented for examination in this application.

Claims 1-20 are rejected.

Applicant's remarks filed 8/18/2009 have been fully considered but they are not persuasive. Therefore, the rejections from the previous office action are respectfully maintained and restated below,

U.S.C. 112, second paragraph

The following is a quotation of the second paragraph of 35 U.S.C. 112:
The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claims 1, 8 and 15, the recitation "a storage capacity …at least approximately equal.." is not clear. In this instant, the metes and bound of "approximately equal" is not ascertained. Therefore it renders the claims to be indefinite.

All dependent claim(s) are rejected as having the same deficiencies as the claim(s) they depend from.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-6, 8-13 and 15-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stoye (US Pat. 6754899) in view of Fischer et al (US Pat. 6438672) and Gappisch et al (US Pub. 2003/0033490).

As in claim 1, Stoye discloses a data access apparatus comprising: an external memory unit for storing data (Fig 1, col. 2 lines 25-30, external memory 16), wherein the external memory unit has a second time cycle for performing a task; and a control unit couples with the external memory unit via a memory bus (Fig 1 IOP's or PP's memory access logic corresponding to the claim's control unit, coupling to memory bus 14 to process tasks relates to data of memory), and a control unit including: a microprocessor unit, having a first time cycle to perform a microprocessor operating (Fig 1 12 PP protocol processor, operating at a first clock cycle, requiring to synchronizing its operations with memory that operating at a second clock cycle, col. 1 line 65 to col. 2

line 3; Examiner note: IOP or PP can be viewed as claim's microprocessor unit, col. 1 lines 17-25); and a memory interface (Fig 1, IOP PP logic to interface with memory 15),

wherein when the microprocessor unit attempts to access the data segment storing flow control parameters and numerical arithmetic from the external memory unit (col. 1 lines 22-25, PP access the code, data, flow tables) an access request signal issued from the control unit associating with the microprocessor unit (PP) against another device (IOP) for accessing the external memory unit is directed to the external memory unit and the first time cycle is suspended until an indicating that of the microprocessor unit may access the data segment of the external memory (col. 1 lines 33-37, 43-51, both PP and IOP access the shared memory 15, the PP must wait until the other processor, i.e IOP completes its memory access),

a memory system including the internal memory unit is accessible only by the processor unit (col. 3 lines 45-56, PP or IOP have private memory);

Stoye does not expressly disclose the claim's details associating with the capacity of internal memory unit and transforming addresses. However, Fisher discloses a memory interface control unit (Fig 1 102 memory aliasing module) configured to correspondingly transform an internal data access address of an internal memory unit to a data address of the external memory unit , thereby enabling the microprocessor unit (Fig 1 104 processor) issuing the internal data access address to access data from the external memory unit via the memory interface control unit (Fig 1, Fig 3, col. 6 lines 10-37, memory aliasing module 102 allows processor 104 to access memory blocks 110), the external memory unit includes a data segment configured to

store flow control parameters and numerical arithmetic of the microprocessor unit that were original stored in the internal memory unit (col. 6 line 45 to col. 7 line 6, storing data of internal memory 106 to memory aliasing module; Examiner notes; the code and data of the internal memory represents flow parameters and numeric arithmetic of the processor), wherein a storage capacity of the data segment included in the external memory unit is substantially equal to a storage capacity of the internal memory unit (col. 6 line 45 to col. 7 line 6, storing code and data portion/unit that were stored in ROM or RAM of module 106 to SDRAM portion/unit, any size of data portion/unit in RAM can be mapped over to corresponding another data portion/unit in SDRAM. The another portion has the same size as the data portion of RAM, see col. 6 lines 50-67). It would have been obvious to one of ordinary skill in the art at the time of invention to include the memory cache/alias method as suggested by Fisher in Stoye's system to store code of internal memory to the memory alias module for fast access and thereby further improve the performance of the overall system.

Stoye and Fisher do not expressly disclose the claim's details associating with the suspending cycle. However, Gappisch discloses a synchronizing method includes the first time cycle is suspended until an acknowledge signal indicating that of the microprocessor can continue (Fig 3, wait_timer provides signals that suspend a processor cycles accessing the flash memory and subsequently allowing the processor cycles to access the device). It would have been obvious to one of ordinary skill in the art at the time of invention to include the synchronizing method as suggested by Gappisch in Stoye's system modified by Fischer thereby allow synchronizing of

independent processors efficiently and thus improve the overall performance of the system (abstract).

As in claim 2, Stoye and Fisher do not expressly disclose the claim's aspect of longer cycles. However, Gappisch further discloses wherein the first time cycle is longer that the second time cycle (Fig3, synchronize independent processors and memory devices with different clocks frequencies; Examiner note: it is commonly known in the art that processors are running at a higher clock frequency that the memory devices). It would have been obvious to one of ordinary skill in the art at the time of invention to adopt teaching of Gappisch in Stoye's system modified by Fisher for the same reasons stated above.

As in claim 3, Stoye discloses wherein the first time cycle is revived from suspending when the second time cycle is finished (col. 1 lines 33-37, 43-51, both PP and IOP access the shared memory 15, the PP must wait until the other processor, i.e IOP completes its memory access, then PP accesses the memory).

As in claim 4, Stoye discloses wherein the duration suspending the first time cycle is a time when the external memory unit finishes a current task (col. 1 lines 33-37, 43-51, both PP and IOP access the shared memory 15, the PP must wait until the other processor, i.e IOP completes its memory access, and then PP accesses the memory).

As in claim 5, Stoye discloses wherein the external memory unit is dynamic random access memory (col. 2 lines 30-50 discloses in an embodiment, the sharing memory is DRAM).

As in claim 6, Stoye discloses wherein a capacity of the data segment of the external memory unit is smaller that a capacity of the external memory unit. (col. 1 lines 21-25, the external memory contains segments that store PP processor codes, data, data buffers, multiple data structures, multiple flow tables and data structures shared by the IOP and the PP processors. Therefore, the external memory not only contains data segments corresponding to the PP processor, but it also contain data buffers for IOP processor such that IOP processor can use to store data being received from an external peripheral device, col. 1 lines 40-43).

As in claim 8, Stoye discloses a control unit for accessing data from an external memory unit (Fig 1, col. 2 lines 25-30, external memory 16), having a second time cycle, via a memory bus in a system (Fig 1 IOP's or PP's memory access logic corresponding to the claim's control unit, coupling to memory bus 14 to process tasks relates to data of memory), the control unit comprising: a microprocessor unit , having a first time cycle, configured to perform a microprocessor operation (Fig 1 12 PP protocol processor, operating at a first clock cycle, requiring to synchronizing its operations with memory that operating at a second clock cycle, col. 1 line 65 to col. 2 line 3; Examiner note: IOP or PP can be viewed as claim's microprocessor unit, col. 1 lines 17-25);

wherein when the microprocessor unit attempts to access the data segment storing flow control parameters and numerical arithmetic from the external memory unit col. 1 lines 22-25, PP access the code, data, flow tables), the access request signal issued from the control unit associated with the microprocessor unit (PP) against another device (IOP) accessing the external memory unit is directed to the external

memory unit, and the first time cycle is suspended until an indicating that the microprocessor unit may access the data segment of the external memory (col. 1 lines 33-37, 43-51, both PP and IOP access the shared memory 15, the PP must wait until the other processor, i.e IOP completes its memory access);

if the microprocessor unit attempts to access data from the external memory unit via the memory interface, the control unit is operable to send an access request signal to the external memory unit (the memory access logic of PP provides memory request to memory 15 on behalf of the PP),

wherein the internal memory unit is accessible by the microprocessor unit (col. 3 lines 45-56, PP or IOP have private memory);

Stoye does not expressly disclose the claim's details associating with the original storing of internal memory unit and transforming addresses. However, Fisher discloses a memory interface control unit (Fig 1 102 memory aliasing module) for configured to correspondingly transform an internal data access address of an internal memory unit to a data address of the external memory unit, thereby enabling the microprocessor unit (Fig 1 104 processor) issuing the internal data access address to access data from the external memory unit via the memory interface control unit (Fig 1, Fig 3, col. 6 lines 10-37, memory aliasing module 102 allows processor 104 to access memory blocks 110); wherein a capacity of the external memory unit is at least approximately equal to a capacity of the internal memory unit (col. 6 line 45 to col. 7 line 6, storing code and data portion/unit that were stored in ROM or RAM of module 106 to SDRAM portion/unit, any size of data portion/unit in RAM can be mapped over to corresponding another data

portion/unit in SDRAM. The another portion has the same size as the data portion of RAM, see col. 6 lines 50-67);

Wherein the external memory unit includes a data segment configured to store flow control parameters and numerical arithmetic of the microprocessor unit that were originally stored in the internal memory unit (col. 6 line 45 to col. 7 line 6, storing data of internal memory 106 to memory aliasing module; Examiner notes; the code and data of the internal memory represents flow parameters and numeric arithmetic of the processor). It would have been obvious to one of ordinary skill in the art at the time of invention to include the memory cache/alias method as suggested by Fisher in Stoye's system to store code of internal memory to the memory alias module for fast access and thereby further improve the performance of the overall system.

Stoye and Fisher do not expressly disclose the claim's details associating with the suspending cycle. However, Gappisch discloses a synchronizing method includes the first time cycle is suspended until an acknowledge signal indicating that of the microprocessor can continue (Fig 3, wait_timer provides signals that suspend a processor cycles accessing the flash memory and subsequently allowing the processor cycles to access the device). It would have been obvious to one of ordinary skill in the art at the time of invention to include the synchronizing method as suggested by Gappisch in Stoye's system modified by Fischer thereby allow synchronizing of independent processors efficiently and thus improve the overall performance of the system (abstract).

As in claim 9, Stoye and Fisher do not expressly disclose the claim's aspect of longer cycles. However, Gappisch further discloses wherein the first time cycle is longer that the second time cycle (Fig3, synchronize independent processors and memory devices with different clocks frequencies; Examiner note: it is commonly known in the art that processors are running at a higher clock frequency that the memory devices). It would have been obvious to one of ordinary skill in the art at the time of invention to adopt teaching of Gappisch in Stoye's system modified by Fisher for the same reasons stated above.

As in claim 10, Stoye discloses wherein the first time cycle is revived from suspending when the second time cycle is finished (col. 1 lines 33-37, 43-51, both PP and IOP access the shared memory 15, the PP must wait until the other processor, i.e IOP completes its memory access, then PP accesses the memory).

As in claim 11, Stoye discloses wherein the duration between the first time cycle suspended and revived is a time when the external memory unit finishes a current task (col. 1 lines 33-37, 43-51, both PP and IOP access the shared memory 15, the PP must wait until the other processor, i.e IOP completes its memory access, then PP accesses the memory).

As in claim 12, Stoye discloses wherein the external memory unit is a DRAM (col. 2 lines 30-50 discloses in an embodiment, the sharing memory is DRAM).

As in claim 13, Stoye discloses wherein a capacity of the data segment of the external memory unit is smaller than a capacity of the external memory unit (col. 1 lines 21-25, the external memory contains segments that store PP processor codes, data,

data buffers, multiple data structures, multiple flow tables and data structures shared by the IOP and the PP processors. Therefore, the external memory not only contains data segments corresponding to the PP processor, but it also contain data buffers for IOP processor such that IOP processor can use to store data being received from an external peripheral device, col. 1 lines 40-43).

As in claim 15, Stoye discloses a data access method used in a control unit for accessing data in an external memory unit (Fig 1, col. 2 lines 25-30, external memory 16), said method comprising:

wherein the access request signal issued from the control unit associated with the microprocessor unit against another device accessing the external memory unit is directed to the external memory unit (col. 1 lines 33-37, 43-51, both PP and IOP access the shared memory 15);

wherein the internal memory unit is accessible only by the microprocessor unit (col. 3 lines 45-56, PP or IOP have private memory);

Stoye does not expressly disclose the claim's details associating with the capacity of internal memory unit and transforming addresses. However, Fisher discloses correspondingly transforming an internal data access address of an internal memory unit to a data address of the external memory unit, thereby enable a microprocessor unit (Fig 1 104 processor) issuing the internal data access to access data from the external memory unit (Fig 1, Fig 3, col. 6 lines 10-37, memory aliasing module 102 allows processor 104 to access memory blocks 110), wherein the data segment stores flow control parameters and numerical arithmetic of the microprocessor

unit that were originally stored in the internal memory unit (col. 6 line 45 to col. 7 line 6, storing data of internal memory 106 to memory aliasing module; Examiner note: the code and data of the internal memory represents flow parameters and numeric arithmetic of the processor), further wherein a storage capacity of the data segment is at least approximately equal to a storage capacity of the internal memory unit (col. 6 line 45 to col. 7 line 6, storing code and data portion/unit that were stored in ROM or RAM of module 106 to SDRAM portion/unit, any size of data portion/unit in RAM can be mapped over to corresponding another data portion/unit in SDRAM. The another portion has the same size as the data portion of RAM, see col. 6 lines 50-67). It would have been obvious to one of ordinary skill in the art at the time of invention to include the memory cache/alias method as suggested by Fisher in Stoye's system to store code of internal memory to the memory alias module for fast access and thereby further improve the performance of the overall system.

Stoye and Fisher do not expressly disclose the claim's details associating with the suspending cycle. However, Gappisch discloses suspending a first time clock used by the microprocessor of the control unit when the microprocessor sends an access request signal for accessing a data segment included in the external memory unit (Fig 3, wait_timer provides signals, i.e activate wait signal that suspend a processor cycles accessing the flash memory) and subsequently in-activate wait signal allowing the processor cycles to access the device); and reviving the first time when an indicating that the microprocessor unit may access the data segment of the external memory unit is received (Fig 3, wait_timer provides signals, and subsequently in-activate wait signal

allowing the processor cycles to access the device). It would have been obvious to one of ordinary skill in the art at the time of invention to include the synchronizing method as suggested by Gappisch in Stoye's system modified by Fischer thereby allow synchronizing of independent processors efficiently and thus improve the overall performance of the system (abstract).

As in claim 16, Stoye discloses wherein the external memory unit has a second time cycle which is a time for accessing data stored in the external memory unit (IOP or PP accessing the memory 15).

As in claim 17, Stoye and Fisher do not expressly disclose the claim's aspect of longer cycles. However, Gappisch further discloses wherein the first time cycle is longer that the second time cycle (Fig3, synchronize independent processors and memory devices with different clocks frequencies).). It would have been obvious to one of ordinary skill in the art at the time of invention to adopt teaching of Gappisch in Stoye's system modified by Fisher for the same reasons stated above.

As in claim 18, Stoye discloses wherein duration of the first time cycle between being suspended and being revived is a time of the second time cycle being finished (col. 1 lines 33-37, 43-51, both PP and IOP access the shared memory 15, the PP must wait until the other processor, i.e IOP completes its memory access, then PP accesses the memory).

As in claim 19, Stoye discloses the external memory unit performs a current task when suspending the first time cycle, and after finishing the current task, reviving the first time cycle immediately (col. 1 lines 33-37, 43-51, both PP and IOP access the

shared memory 15, the PP must wait until the other processor, i.e IOP completes its memory access, then PP accesses the memory).

Claims 7, 14 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stoye (US Pat. 6754899), Fischer et al (US Pat. 6438672) and Gappisch et al (US Pub. 2003/0033490) as applied above and further in view of Nishizawa et al (US Pub. 2002/0098886).

As in claim 7, Stoye discloses data access device including IOP for controlling i/o devices. Stoye, Fisher and Gappisch do not expressly disclose the claim's aspect of optical-electronic devices. However, Nishizawa discloses a system includes IOP and wherein data access apparatus could be applied to an optical-electronic system and which is selected from CD-ROM, CD-RW, CD-RW, DVD+/-Rom, and DVD +/- RW (par. 49). It would have been obvious to one of ordinary skill in the art at the time of invention to apply IOP for optical-electronic devices as suggested by Nishizawa in Stoye's system modified by Fisher and Gappisch thereby further allowing visual and audio application in the CD-ROM DVD-ROM to be processed in an efficiently manner (abstract).

As in claim 14, Stoye discloses data access device including IOP for controlling i/o devices. Stoye, Fisher and Gappisch do not expressly disclose the claim's aspect of optical-electronic devices. However, Nishizawa discloses wherein the optical-electronic is selected from: a CD-ROM, a CD-RW, a DVD+/-ROM, and DVD+/-RW (par. 49). It would have been obvious to one of ordinary skill in the art at the time of invention to apply IOP for optical-electronic devices as suggested by Nishizawa in Stoye's system modified by Fisher and Gappisch and thereby further allowing visual and audio

application in the CD-ROM DVD-ROM to be processed in an efficiently manner (abstract).

As in claim 20, Stoye discloses data access device including IOP for controlling i/o devices. Stoye, Fisher and Gappisch do not expressly disclose the claim's aspect of optical-electronic devices. However, Nishizawa discloses a system includes IOP and wherein data access apparatus could be applied to an optical-electronic system and which is selected from CD-ROM, CD-RW, CD-RW, DVD+/-Rom, and DVD +/- RW (par. 49). It would have been obvious to one of ordinary skill in the art at the time of invention to apply IOP for optical-electronic devices as suggested by Nishizawa in Stoye's system modified by Fisher and Gappisch thereby further allowing visual and audio application in the CD-ROM DVD-ROM to be processed in an efficiently manner (abstract).

Response to Arguments

Applicant's arguments in response to the last office action has been fully considered but they are not persuasive. Examiner respectfully traverses Applicant's arguments for the following reasons:

A) With regard to the amending of claims 1, 8 and 15 to recite "..at least approximately equal..". Examiner maintains that the terminology is not clear and cause indefinite as stated in the 35 U.S.C. 112 second paragraph rejection sections.

B) Regarding Applicant's arguments at pages 8-10 for the rejections of claims 1-6, 8-13 and 15-19 under 35 U.S.C 103(a), the arguments are not persuasive.

Applicant argues

> "Applicant's technology is directed to enabling a chip to access data that is stored in memory that is external to the chip, thereby reducing manufacturing cost for the chip. Because applicant's technology stores in the external memory "flow control parameters and numerical arithmetic of the microprocessor unit that were originally stored in the internal memory," it employs external memory that has storage capacity "at least approximately equal to a storage capacity of the internal memory unit."
>
> In complete contrast, Fischer's technique has absolutely no need for a spare memory storage capacity that is "at least approximately equal to a storage capacity of the internal memory unit" because spare (or cache) memory holds "a small subset of data stored in the main memory. The processor needs only a certain (sic, a) small amount of the data in the main memory to execute individual instructions for a particular application." (Fischer, 1:53-54.).

In response, Applicant admits that Fischer teaches of an external memory to store instructions and data to execute a particular application (col. 1 lines 51-56). In addition, a processor stores in its internal memory several set of instructions and data of several applications being run. This aggregated data constitutes a large amount of data that causes thrashing of cache memory (col. 2 lines 45-67). Thus Fisher teaches that data instead of storing in internal memory, i.e the claim's "original stored", is stored in external memory and processor requests is directed to data stored in the external memory. Of course this aggregated data can be any size larger and or equal to the

internal data to accommodate for any information which is "original" stored in the internal data (col. 6 lines 55-67, the external memory to store any repeated information that was "original" stored in the internal memory, “any repeatedly referenced information ..variable common code segments,, routine.. may be overlaid by the methods..").

Finally, it’s noted that the claims merely claims a memory unit, which can be reasonably interpreted as an amount of data. And Fisher clearly teaches of having external memory to store any data amount that was stored in the internal memory. Thus the external memory unit/amount is equal the internal unit/amount.

Applicant further argues,

“.. In Fischer, the memory aliasing module intercepts the data path between the addressable circuits (e.g., memory) and the processor and, when the most significant bit (MSB) of the address is high (e.g., 1), Fischer's technique redirects the memory to the spare memory. (Fischer, 8:7-19.) Because the most significant bit of the address is used to determine whether or not the spare memory is to be referenced, the capacity of the spare memory can be no more than half the capacity of the main memory. Thus, Fischer teaches away because the external (spare) memory used by Fischer's technique must be significantly smaller than its main memory. Moreover, modifying Fischer's technique to use external memory that is the same size as the internal memory would destroy how Fischer's technique operates. The Office Action points to no other reference as teaching or suggesting this feature. Accordingly, claims 1-7

patentably define over the references, both alone and in combination. Applicant respectfully requests reconsideration"

In response, Applicant mischaracterizes Fishcher's teaching of using the address bit to address the external memory and concludes that the most significant address bit somehow "..teaching away"" and ".capacity of the external spare memory..must be smaller than its main memory. The argument is confusing and appears lacks of support.

Examiner submits that there is no disclosure in the current application that requires the external spare memory, i.e temporary segment of the invention, must be smaller than the external memory, i.e DRAM of the invention. In fact, the specification's page 5 lines 18-21 clearly disclose the temporary segment 210 is a segment of the external memory DRAM. Thus the temporary segment is a part of the external memory and is smaller that the external memory. In other words, the argument contradicts with the disclosure, and therefore the argument is improper and not persuasive.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 36 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

When responding to the office action, Applicant is advised to provide the examiner with the paragraph numbers, and/or line numbers and page numbers in the application to assist examiner to locate the appropriate paragraphs.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Duc T. Doan whose telephone number is 571-272-4171. The examiner can normally be reached on M-F 8:00 AM 05:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on 571-272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

/Sanjiv Shah/
Supervisory Patent Examiner, Art Unit 2185